---------- Begin Simulation Statistics ----------

sim\_seconds 0.144932 # Number of seconds simulated

sim\_ticks 144932423500 # Number of ticks simulated

final\_tick 144932423500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)

sim\_freq 1000000000000 # Frequency of simulated ticks

host\_inst\_rate 313466 # Simulator instruction rate (inst/s)

host\_op\_rate 313466 # Simulator op (including micro ops) rate (op/s)

host\_tick\_rate 104140293 # Simulator tick rate (ticks/s)

host\_mem\_usage 644876 # Number of bytes of host memory used

host\_seconds 1391.70 # Real time elapsed on the host

sim\_insts 436251113 # Number of instructions simulated

sim\_ops 436251113 # Number of ops (including micro ops) simulated

system.voltage\_domain.voltage 1 # Voltage in Volts

system.clk\_domain.clock 1000 # Clock period in ticks

system.mem\_ctrls.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.mem\_ctrls.bytes\_read::.cpu.inst 88260736 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::.cpu.data 188992 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::total 88449728 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::.cpu.inst 88260736 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::total 88260736 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_written::.writebacks 24128 # Number of bytes written to this memory

system.mem\_ctrls.bytes\_written::total 24128 # Number of bytes written to this memory

system.mem\_ctrls.num\_reads::.cpu.inst 1379074 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::.cpu.data 2953 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::total 1382027 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_writes::.writebacks 377 # Number of write requests responded to by this memory

system.mem\_ctrls.num\_writes::total 377 # Number of write requests responded to by this memory

system.mem\_ctrls.bw\_read::.cpu.inst 608978542 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::.cpu.data 1304001 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::total 610282543 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::.cpu.inst 608978542 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::total 608978542 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_write::.writebacks 166478 # Write bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_write::total 166478 # Write bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.writebacks 166478 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.inst 608978542 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::.cpu.data 1304001 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::total 610449021 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.avgPriority\_.writebacks::samples 474447.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.inst::samples 361731.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.avgPriority\_.cpu.data::samples 2812.00 # Average QoS priority value for accepted requests

system.mem\_ctrls.priorityMinLatency 0.000000018750 # per QoS priority minimum request to response latency (s)

system.mem\_ctrls.priorityMaxLatency 0.149104867750 # per QoS priority maximum request to response latency (s)

system.mem\_ctrls.numReadWriteTurnArounds 28619 # Number of turnarounds from READ to WRITE

system.mem\_ctrls.numWriteReadTurnArounds 28619 # Number of turnarounds from WRITE to READ

system.mem\_ctrls.numStayReadState 2073133 # Number of times bus staying in READ state

system.mem\_ctrls.numStayWriteState 446870 # Number of times bus staying in WRITE state

system.mem\_ctrls.readReqs 1382029 # Number of read requests accepted

system.mem\_ctrls.writeReqs 1378939 # Number of write requests accepted

system.mem\_ctrls.readBursts 1382029 # Number of DRAM read bursts, including those serviced by the write queue

system.mem\_ctrls.writeBursts 1378939 # Number of DRAM write bursts, including those merged in the write queue

system.mem\_ctrls.bytesReadDRAM 23330752 # Total number of bytes read from DRAM

system.mem\_ctrls.bytesReadWrQ 65119104 # Total number of bytes read from write queue

system.mem\_ctrls.bytesWritten 30363072 # Total number of bytes written to DRAM

system.mem\_ctrls.bytesReadSys 88449856 # Total read bytes from the system interface side

system.mem\_ctrls.bytesWrittenSys 88252096 # Total written bytes from the system interface side

system.mem\_ctrls.servicedByWrQ 1017486 # Number of DRAM read bursts serviced by the write queue

system.mem\_ctrls.mergedWrBursts 904492 # Number of DRAM write bursts merged with an existing one

system.mem\_ctrls.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write

system.mem\_ctrls.perBankRdBursts::0 96197 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::1 9410 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::2 106707 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::3 2272 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::4 4204 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::5 2307 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::6 102055 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::7 4888 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::8 466 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::9 509 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::10 439 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::11 80 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::12 17554 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::13 21 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::14 17108 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::15 326 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::0 118355 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::1 9907 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::2 116854 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::3 2884 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::4 4251 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::5 1885 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::6 162334 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::7 8094 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::8 336 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::9 96 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::10 20 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::11 55 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::12 26013 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::13 13 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::14 18168 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::15 5158 # Per bank write bursts

system.mem\_ctrls.numRdRetry 0 # Number of times read queue was full causing retry

system.mem\_ctrls.numWrRetry 0 # Number of times write queue was full causing retry

system.mem\_ctrls.totGap 144932409000 # Total gap between requests

system.mem\_ctrls.readPktSize::0 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::1 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::2 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::3 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::4 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::5 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::6 1382029 # Read request sizes (log2)

system.mem\_ctrls.writePktSize::0 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::1 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::2 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::3 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::4 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::5 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::6 1378939 # Write request sizes (log2)

system.mem\_ctrls.rdQLenPdf::0 341214 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::1 21969 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::2 1146 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::3 196 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::4 15 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::5 3 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::6 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::7 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::8 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::9 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::10 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::11 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::12 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::13 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::14 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::15 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::16 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::17 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::18 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::19 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::20 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::21 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::23 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::24 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::25 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::26 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::27 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::28 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::29 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::30 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::31 0 # What read queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::0 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::1 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::2 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::3 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::4 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::5 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::6 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::7 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::8 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::9 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::10 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::11 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::12 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::13 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::14 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::15 4775 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::16 5559 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::17 24012 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::18 28163 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::19 30599 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::20 29421 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::21 29445 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::22 29348 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::23 32380 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::24 29532 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::25 29017 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::26 28812 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::27 29710 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::28 28838 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::29 28707 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::30 28669 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::31 28671 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::32 28671 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::33 51 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::34 25 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::35 16 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::36 9 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::37 2 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::38 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::39 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::41 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::42 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::43 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::44 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::45 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::46 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::47 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::48 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::49 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::50 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::51 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::52 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::53 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::54 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::55 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::56 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::57 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::58 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::59 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::60 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::61 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::62 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::63 0 # What write queue length does an incoming req see

system.mem\_ctrls.bytesPerActivate::samples 154118 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::mean 348.369327 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::gmean 246.581551 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::stdev 273.657550 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::0-127 29043 18.84% 18.84% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::128-255 37987 24.65% 43.49% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::256-383 23662 15.35% 58.85% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::384-511 22588 14.66% 73.50% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::512-639 14197 9.21% 82.71% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::640-767 9161 5.94% 88.66% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::768-895 5721 3.71% 92.37% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::896-1023 4308 2.80% 95.17% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::1024-1151 7451 4.83% 100.00% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::total 154118 # Bytes accessed per row activation

system.mem\_ctrls.rdPerTurnAround::samples 28619 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::mean 12.737482 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::gmean 12.380431 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::stdev 3.598240 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::0-15 24314 84.96% 84.96% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::16-31 4297 15.01% 99.97% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::32-47 4 0.01% 99.99% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::48-63 2 0.01% 99.99% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::80-95 1 0.00% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::384-399 1 0.00% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::total 28619 # Reads before turning the bus around for writes

system.mem\_ctrls.wrPerTurnAround::samples 28619 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::mean 16.577204 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::gmean 16.532758 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::stdev 1.277738 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::16 22898 80.01% 80.01% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::17 452 1.58% 81.59% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::18 2414 8.43% 90.02% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::19 855 2.99% 93.01% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::20 1472 5.14% 98.16% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::21 402 1.40% 99.56% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::22 113 0.39% 99.95% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::23 12 0.04% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::30 1 0.00% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::total 28619 # Writes before turning the bus around for reads

system.mem\_ctrls.masterReadBytes::.cpu.inst 23150784 # Per-master bytes read from memory

system.mem\_ctrls.masterReadBytes::.cpu.data 179968 # Per-master bytes read from memory

system.mem\_ctrls.masterWriteBytes::.writebacks 30363072 # Per-master bytes write to memory

system.mem\_ctrls.masterReadRate::.cpu.inst 159735022.991594433784 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterReadRate::.cpu.data 1241737.325947633944 # Per-master bytes read from memory rate (Bytes/sec)

system.mem\_ctrls.masterWriteRate::.writebacks 209498132.072565555573 # Per-master bytes write to memory rate (Bytes/sec)

system.mem\_ctrls.masterReadAccesses::.cpu.inst 1379075 # Per-master read serviced memory accesses

system.mem\_ctrls.masterReadAccesses::.cpu.data 2954 # Per-master read serviced memory accesses

system.mem\_ctrls.masterWriteAccesses::.writebacks 1378939 # Per-master write serviced memory accesses

system.mem\_ctrls.masterReadTotalLat::.cpu.inst 13851038250 # Per-master read total memory access latency

system.mem\_ctrls.masterReadTotalLat::.cpu.data 144172500 # Per-master read total memory access latency

system.mem\_ctrls.masterWriteTotalLat::.writebacks 4025565287250 # Per-master write total memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.inst 10043.72 # Per-master read average memory access latency

system.mem\_ctrls.masterReadAvgLat::.cpu.data 48805.86 # Per-master read average memory access latency

system.mem\_ctrls.masterWriteAvgLat::.writebacks 2919320.79 # Per-master write average memory access latency

system.mem\_ctrls.totQLat 7160029500 # Total ticks spent queuing

system.mem\_ctrls.totMemAccLat 13995210750 # Total ticks spent from burst creation until serviced by the DRAM

system.mem\_ctrls.totBusLat 1822715000 # Total ticks spent in databus transfers

system.mem\_ctrls.avgQLat 19641.11 # Average queueing delay per DRAM burst

system.mem\_ctrls.avgBusLat 5000.00 # Average bus latency per DRAM burst

system.mem\_ctrls.avgMemAccLat 38391.11 # Average memory access latency per DRAM burst

system.mem\_ctrls.avgRdBW 160.98 # Average DRAM read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBW 209.50 # Average achieved write bandwidth in MiByte/s

system.mem\_ctrls.avgRdBWSys 610.28 # Average system read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBWSys 608.92 # Average system write bandwidth in MiByte/s

system.mem\_ctrls.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s

system.mem\_ctrls.busUtil 2.89 # Data bus utilization in percentage

system.mem\_ctrls.busUtilRead 1.26 # Data bus utilization in percentage for reads

system.mem\_ctrls.busUtilWrite 1.64 # Data bus utilization in percentage for writes

system.mem\_ctrls.avgRdQLen 1.02 # Average read queue length when enqueuing

system.mem\_ctrls.avgWrQLen 28.06 # Average write queue length when enqueuing

system.mem\_ctrls.readRowHits 281069 # Number of row buffer hits during reads

system.mem\_ctrls.writeRowHits 403768 # Number of row buffer hits during writes

system.mem\_ctrls.readRowHitRate 77.10 # Row buffer hit rate for reads

system.mem\_ctrls.writeRowHitRate 85.10 # Row buffer hit rate for writes

system.mem\_ctrls.avgGap 52493.33 # Average gap between requests

system.mem\_ctrls.pageHitRate 81.63 # Row buffer hit rate, read and write combined

system.mem\_ctrls\_0.actEnergy 926086560 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_0.preEnergy 492211500 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_0.readEnergy 2342198460 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_0.writeEnergy 2216224080 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_0.refreshEnergy 2971169760.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_0.actBackEnergy 6665222040 # Energy for active background per rank (pJ)

system.mem\_ctrls\_0.preBackEnergy 66836640 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_0.actPowerDownEnergy 10287436950 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_0.prePowerDownEnergy 115016160 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_0.selfRefreshEnergy 25763134320 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_0.totalEnergy 51845536470 # Total energy per rank (pJ)

system.mem\_ctrls\_0.averagePower 357.722138 # Core power per rank (mW)

system.mem\_ctrls\_0.totalIdleTime 130143183250 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_0.memoryStateTime::IDLE 27450000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::REF 1256840000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::SREF 107281961500 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::PRE\_PDN 299402250 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT 13504950250 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT\_PDN 22561819500 # Time in different power states

system.mem\_ctrls\_1.actEnergy 174387360 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_1.preEnergy 92666310 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_1.readEnergy 260624280 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_1.writeEnergy 260263980 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_1.refreshEnergy 2948428080.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_1.actBackEnergy 9451274310 # Energy for active background per rank (pJ)

system.mem\_ctrls\_1.preBackEnergy 149630880 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_1.actPowerDownEnergy 5392816170 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_1.prePowerDownEnergy 1695921120 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_1.selfRefreshEnergy 25824811620 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_1.totalEnergy 46250824110 # Total energy per rank (pJ)

system.mem\_ctrls\_1.averagePower 319.119925 # Core power per rank (mW)

system.mem\_ctrls\_1.totalIdleTime 123816008250 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_1.memoryStateTime::IDLE 251862000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::REF 1247220000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::SREF 107573469250 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::PRE\_PDN 4415856000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT 19617333250 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT\_PDN 11826683000 # Time in different power states

system.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.cpu.branchPred.lookups 70762922 # Number of BP lookups

system.cpu.branchPred.condPredicted 51581164 # Number of conditional branches predicted

system.cpu.branchPred.condIncorrect 1463644 # Number of conditional branches incorrect

system.cpu.branchPred.BTBLookups 52408291 # Number of BTB lookups

system.cpu.branchPred.BTBHits 46229129 # Number of BTB hits

system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.

system.cpu.branchPred.BTBHitPct 88.209572 # BTB Hit Percentage

system.cpu.branchPred.usedRAS 6339997 # Number of times the RAS was used to get a target.

system.cpu.branchPred.RASInCorrect 33 # Number of incorrect RAS predictions.

system.cpu.branchPred.indirectLookups 1670120 # Number of indirect predictor lookups.

system.cpu.branchPred.indirectHits 1639367 # Number of indirect target hits.

system.cpu.branchPred.indirectMisses 30753 # Number of indirect misses.

system.cpu.branchPredindirectMispredicted 132 # Number of mispredicted indirect branches.

system.cpu\_voltage\_domain.voltage 1 # Voltage in Volts

system.cpu\_clk\_domain.clock 500 # Clock period in ticks

system.cpu.dtb.fetch\_hits 0 # ITB hits

system.cpu.dtb.fetch\_misses 0 # ITB misses

system.cpu.dtb.fetch\_acv 0 # ITB acv

system.cpu.dtb.fetch\_accesses 0 # ITB accesses

system.cpu.dtb.read\_hits 75009048 # DTB read hits

system.cpu.dtb.read\_misses 57 # DTB read misses

system.cpu.dtb.read\_acv 0 # DTB read access violations

system.cpu.dtb.read\_accesses 75009105 # DTB read accesses

system.cpu.dtb.write\_hits 40281259 # DTB write hits

system.cpu.dtb.write\_misses 8 # DTB write misses

system.cpu.dtb.write\_acv 0 # DTB write access violations

system.cpu.dtb.write\_accesses 40281267 # DTB write accesses

system.cpu.dtb.data\_hits 115290307 # DTB hits

system.cpu.dtb.data\_misses 65 # DTB misses

system.cpu.dtb.data\_acv 0 # DTB access violations

system.cpu.dtb.data\_accesses 115290372 # DTB accesses

system.cpu.itb.fetch\_hits 71123790 # ITB hits

system.cpu.itb.fetch\_misses 309 # ITB misses

system.cpu.itb.fetch\_acv 0 # ITB acv

system.cpu.itb.fetch\_accesses 71124099 # ITB accesses

system.cpu.itb.read\_hits 0 # DTB read hits

system.cpu.itb.read\_misses 0 # DTB read misses

system.cpu.itb.read\_acv 0 # DTB read access violations

system.cpu.itb.read\_accesses 0 # DTB read accesses

system.cpu.itb.write\_hits 0 # DTB write hits

system.cpu.itb.write\_misses 0 # DTB write misses

system.cpu.itb.write\_acv 0 # DTB write access violations

system.cpu.itb.write\_accesses 0 # DTB write accesses

system.cpu.itb.data\_hits 0 # DTB hits

system.cpu.itb.data\_misses 0 # DTB misses

system.cpu.itb.data\_acv 0 # DTB access violations

system.cpu.itb.data\_accesses 0 # DTB accesses

system.cpu.workload.numSyscalls 167539 # Number of system calls

system.cpu.pwrStateResidencyTicks::ON 144932423500 # Cumulative time (in ticks) in various power states

system.cpu.numCycles 289864849 # number of cpu cycles simulated

system.cpu.numWorkItemsStarted 0 # number of work items this cpu started

system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed

system.cpu.fetch.icacheStallCycles 106985522 # Number of cycles fetch is stalled on an Icache miss

system.cpu.fetch.Insts 485507542 # Number of instructions fetch has processed

system.cpu.fetch.Branches 70762922 # Number of branches that fetch encountered

system.cpu.fetch.predictedBranches 54208493 # Number of branches that fetch has predicted taken

system.cpu.fetch.Cycles 122143029 # Number of cycles fetch has run and was not squashing or blocked

system.cpu.fetch.SquashCycles 3128210 # Number of cycles fetch has spent squashing

system.cpu.fetch.MiscStallCycles 272 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs

system.cpu.fetch.PendingTrapStallCycles 1885 # Number of stall cycles due to pending traps

system.cpu.fetch.IcacheWaitRetryStallCycles 138 # Number of stall cycles due to full MSHR

system.cpu.fetch.CacheLines 71123790 # Number of cache lines fetched

system.cpu.fetch.IcacheSquashes 493001 # Number of outstanding Icache misses that were squashed

system.cpu.fetch.rateDist::samples 230694951 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::mean 2.104543 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::stdev 2.903439 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::0 127375434 55.21% 55.21% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::1 16608147 7.20% 62.41% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::2 11906577 5.16% 67.57% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::3 7377736 3.20% 70.77% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::4 16585880 7.19% 77.96% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::5 9134299 3.96% 81.92% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::6 6835028 2.96% 84.88% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::7 9046950 3.92% 88.81% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::8 25824900 11.19% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::min\_value 0 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::max\_value 8 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::total 230694951 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.branchRate 0.244124 # Number of branch fetches per cycle

system.cpu.fetch.rate 1.674945 # Number of inst fetches per cycle

system.cpu.decode.IdleCycles 93066002 # Number of cycles decode is idle

system.cpu.decode.BlockedCycles 44335971 # Number of cycles decode is blocked

system.cpu.decode.RunCycles 80322854 # Number of cycles decode is running

system.cpu.decode.UnblockCycles 11512063 # Number of cycles decode is unblocking

system.cpu.decode.SquashCycles 1458061 # Number of cycles decode is squashing

system.cpu.decode.BranchResolved 45741362 # Number of times decode resolved a branch

system.cpu.decode.BranchMispred 106113 # Number of times decode detected a branch misprediction

system.cpu.decode.DecodedInsts 473926990 # Number of instructions handled by decode

system.cpu.decode.SquashedInsts 140017 # Number of squashed instructions handled by decode

system.cpu.rename.SquashCycles 1458061 # Number of cycles rename is squashing

system.cpu.rename.IdleCycles 97900531 # Number of cycles rename is idle

system.cpu.rename.BlockCycles 1559021 # Number of cycles rename is blocking

system.cpu.rename.serializeStallCycles 17464821 # count of cycles rename stalled for serializing inst

system.cpu.rename.RunCycles 86945678 # Number of cycles rename is running

system.cpu.rename.UnblockCycles 25366839 # Number of cycles rename is unblocking

system.cpu.rename.RenamedInsts 468925614 # Number of instructions processed by rename

system.cpu.rename.ROBFullEvents 166 # Number of times rename has blocked due to ROB full

system.cpu.rename.IQFullEvents 23303171 # Number of times rename has blocked due to IQ full

system.cpu.rename.LQFullEvents 1910 # Number of times rename has blocked due to LQ full

system.cpu.rename.SQFullEvents 1076 # Number of times rename has blocked due to SQ full

system.cpu.rename.RenamedOperands 355854567 # Number of destination operands rename has renamed

system.cpu.rename.RenameLookups 667059654 # Number of register rename lookups that rename has made

system.cpu.rename.int\_rename\_lookups 662734044 # Number of integer rename lookups

system.cpu.rename.fp\_rename\_lookups 3700041 # Number of floating rename lookups

system.cpu.rename.CommittedMaps 337898601 # Number of HB maps that are committed

system.cpu.rename.UndoneMaps 17955966 # Number of HB maps that are undone due to squashing

system.cpu.rename.serializingInsts 1103499 # count of serializing insts renamed

system.cpu.rename.tempSerializingInsts 349294 # count of temporary serializing insts renamed

system.cpu.rename.skidInsts 53330779 # count of insts added to the skid buffer

system.cpu.memDep0.insertedLoads 75795858 # Number of loads inserted to the mem dependence unit.

system.cpu.memDep0.insertedStores 40810776 # Number of stores inserted to the mem dependence unit.

system.cpu.memDep0.conflictingLoads 4254460 # Number of conflicting loads.

system.cpu.memDep0.conflictingStores 1344628 # Number of conflicting stores.

system.cpu.iq.iqInstsAdded 454074670 # Number of instructions added to the IQ (excludes non-spec)

system.cpu.iq.iqNonSpecInstsAdded 476400 # Number of non-speculative instructions added to the IQ

system.cpu.iq.iqInstsIssued 447711764 # Number of instructions issued

system.cpu.iq.iqSquashedInstsIssued 12636 # Number of squashed instructions issued

system.cpu.iq.iqSquashedInstsExamined 18299956 # Number of squashed instructions iterated over during squash; mainly for profiling

system.cpu.iq.iqSquashedOperandsExamined 13028018 # Number of squashed operands that are examined and possibly removed from graph

system.cpu.iq.iqSquashedNonSpecRemoved 276 # Number of squashed non-spec instructions that were removed

system.cpu.iq.issued\_per\_cycle::samples 230694951 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::mean 1.940709 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::stdev 1.748341 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::0 62603671 27.14% 27.14% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::1 40599330 17.60% 44.74% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::2 49909282 21.63% 66.37% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::3 37238310 16.14% 82.51% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::4 21263839 9.22% 91.73% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::5 10023785 4.35% 96.07% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::6 4476212 1.94% 98.01% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::7 3096789 1.34% 99.36% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::8 1483733 0.64% 100.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::min\_value 0 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::max\_value 8 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::total 230694951 # Number of insts issued each cycle

system.cpu.iq.fu\_full::No\_OpClass 0 0.00% 0.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntAlu 234881 4.49% 4.49% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntMult 111261 2.13% 6.62% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntDiv 0 0.00% 6.62% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatAdd 19 0.00% 6.62% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatCmp 9 0.00% 6.62% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatCvt 1 0.00% 6.62% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMult 973 0.02% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMultAcc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatDiv 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMisc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatSqrt 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAdd 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAddAcc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAlu 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdCmp 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdCvt 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMisc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMult 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMultAcc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShift 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShiftAcc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSqrt 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatAdd 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatAlu 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatCmp 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatCvt 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatDiv 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMisc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMult 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMultAcc 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatSqrt 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAes 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAesMix 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha1Hash 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha1Hash2 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha256Hash 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSha256Hash2 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShaSigma2 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShaSigma3 0 0.00% 6.64% # attempts to use FU when none available

system.cpu.iq.fu\_full::MemRead 2716447 51.94% 58.57% # attempts to use FU when none available

system.cpu.iq.fu\_full::MemWrite 1754019 33.54% 92.11% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMemRead 110257 2.11% 94.22% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMemWrite 302389 5.78% 100.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available

system.cpu.iq.FU\_type\_0::No\_OpClass 64668 0.01% 0.01% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntAlu 327516938 73.15% 73.17% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntMult 2408001 0.54% 73.71% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntDiv 0 0.00% 73.71% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatAdd 905578 0.20% 73.91% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatCmp 195493 0.04% 73.95% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatCvt 281616 0.06% 74.01% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMult 206011 0.05% 74.06% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMultAcc 0 0.00% 74.06% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatDiv 60618 0.01% 74.07% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMisc 0 0.00% 74.07% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatSqrt 4370 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAdd 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAddAcc 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAlu 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdCmp 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdCvt 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMisc 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMult 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMultAcc 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShift 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShiftAcc 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSqrt 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatAdd 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatAlu 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatCmp 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatCvt 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatDiv 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMisc 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMult 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMultAcc 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatSqrt 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAes 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAesMix 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha1Hash 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha1Hash2 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha256Hash 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSha256Hash2 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShaSigma2 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShaSigma3 0 0.00% 74.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::MemRead 75121583 16.78% 90.85% # Type of FU issued

system.cpu.iq.FU\_type\_0::MemWrite 39506067 8.82% 99.68% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMemRead 582989 0.13% 99.81% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMemWrite 857832 0.19% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::IprAccess 0 0.00% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::total 447711764 # Type of FU issued

system.cpu.iq.rate 1.544553 # Inst issue rate

system.cpu.iq.fu\_busy\_cnt 5230256 # FU busy when requested

system.cpu.iq.fu\_busy\_rate 0.011682 # FU busy rate (busy events/executed inst)

system.cpu.iq.int\_inst\_queue\_reads 1124758700 # Number of integer instruction queue reads

system.cpu.iq.int\_inst\_queue\_writes 469830991 # Number of integer instruction queue writes

system.cpu.iq.int\_inst\_queue\_wakeup\_accesses 441028900 # Number of integer instruction queue wakeup accesses

system.cpu.iq.fp\_inst\_queue\_reads 6602671 # Number of floating instruction queue reads

system.cpu.iq.fp\_inst\_queue\_writes 3168373 # Number of floating instruction queue writes

system.cpu.iq.fp\_inst\_queue\_wakeup\_accesses 3089472 # Number of floating instruction queue wakeup accesses

system.cpu.iq.vec\_inst\_queue\_reads 0 # Number of vector instruction queue reads

system.cpu.iq.vec\_inst\_queue\_writes 0 # Number of vector instruction queue writes

system.cpu.iq.vec\_inst\_queue\_wakeup\_accesses 0 # Number of vector instruction queue wakeup accesses

system.cpu.iq.int\_alu\_accesses 449369197 # Number of integer alu accesses

system.cpu.iq.fp\_alu\_accesses 3508155 # Number of floating point alu accesses

system.cpu.iq.vec\_alu\_accesses 0 # Number of vector alu accesses

system.cpu.iew.lsq.thread0.forwLoads 4891080 # Number of loads that had data forwarded from stores

system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address

system.cpu.iew.lsq.thread0.squashedLoads 4161528 # Number of loads squashed

system.cpu.iew.lsq.thread0.ignoredResponses 2115 # Number of memory responses ignored because the instruction is squashed

system.cpu.iew.lsq.thread0.memOrderViolation 148373 # Number of memory ordering violations

system.cpu.iew.lsq.thread0.squashedStores 1617988 # Number of stores squashed

system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address

system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding

system.cpu.iew.lsq.thread0.rescheduledLoads 245706 # Number of loads that were rescheduled

system.cpu.iew.lsq.thread0.cacheBlocked 170 # Number of times an access to memory failed due to the cache being blocked

system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle

system.cpu.iew.iewSquashCycles 1458061 # Number of cycles IEW is squashing

system.cpu.iew.iewBlockCycles 1559817 # Number of cycles IEW is blocking

system.cpu.iew.iewUnblockCycles 582 # Number of cycles IEW is unblocking

system.cpu.iew.iewDispatchedInsts 463343784 # Number of instructions dispatched to IQ

system.cpu.iew.iewDispSquashedInsts 584248 # Number of squashed instructions skipped by dispatch

system.cpu.iew.iewDispLoadInsts 75795858 # Number of dispatched load instructions

system.cpu.iew.iewDispStoreInsts 40810776 # Number of dispatched store instructions

system.cpu.iew.iewDispNonSpecInsts 322055 # Number of dispatched non-speculative instructions

system.cpu.iew.iewIQFullEvents 235 # Number of times the IQ has become full, causing a stall

system.cpu.iew.iewLSQFullEvents 255 # Number of times the LSQ has become full, causing a stall

system.cpu.iew.memOrderViolationEvents 148373 # Number of memory order violations

system.cpu.iew.predictedTakenIncorrect 945349 # Number of branches that were predicted taken incorrectly

system.cpu.iew.predictedNotTakenIncorrect 431867 # Number of branches that were predicted not taken incorrectly

system.cpu.iew.branchMispredicts 1377216 # Number of branch mispredicts detected at execute

system.cpu.iew.iewExecutedInsts 445987233 # Number of executed instructions

system.cpu.iew.iewExecLoadInsts 75009105 # Number of load instructions executed

system.cpu.iew.iewExecSquashedInsts 1724531 # Number of squashed instructions skipped in execute

system.cpu.iew.exec\_swp 0 # number of swp insts executed

system.cpu.iew.exec\_nop 8792714 # number of nop insts executed

system.cpu.iew.exec\_refs 115290374 # number of memory reference insts executed

system.cpu.iew.exec\_branches 66131178 # Number of branches executed

system.cpu.iew.exec\_stores 40281269 # Number of stores executed

system.cpu.iew.exec\_rate 1.538604 # Inst execution rate

system.cpu.iew.wb\_sent 444554478 # cumulative count of insts sent to commit

system.cpu.iew.wb\_count 444118372 # cumulative count of insts written-back

system.cpu.iew.wb\_producers 285085842 # num instructions producing a value

system.cpu.iew.wb\_consumers 403398387 # num instructions consuming a value

system.cpu.iew.wb\_rate 1.532157 # insts written-back per cycle

system.cpu.iew.wb\_fanout 0.706710 # average fanout of values written-back

system.cpu.commit.commitSquashedInsts 18510621 # The number of squashed insts skipped by commit

system.cpu.commit.commitNonSpecStalls 476124 # The number of times commit has been forced to stall to communicate backwards

system.cpu.commit.branchMispredicts 1357823 # The number of times a branch was mispredicted

system.cpu.commit.committed\_per\_cycle::samples 227678867 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::mean 1.953774 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::stdev 2.263488 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::0 68903608 30.26% 30.26% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::1 50377363 22.13% 52.39% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::2 60374261 26.52% 78.91% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::3 8449340 3.71% 82.62% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::4 10608428 4.66% 87.28% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::5 3164654 1.39% 88.67% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::6 6076767 2.67% 91.34% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::7 4154001 1.82% 93.16% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::8 15570445 6.84% 100.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::min\_value 0 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::max\_value 8 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::total 227678867 # Number of insts commited each cycle

system.cpu.commit.committedInsts 444833056 # Number of instructions committed

system.cpu.commit.committedOps 444833056 # Number of ops (including micro ops) committed

system.cpu.commit.swp\_count 0 # Number of s/w prefetches committed

system.cpu.commit.refs 110827118 # Number of memory references committed

system.cpu.commit.loads 71634330 # Number of loads committed

system.cpu.commit.membars 154292 # Number of memory barriers committed

system.cpu.commit.branches 65078964 # Number of branches committed

system.cpu.commit.vec\_insts 0 # Number of committed Vector instructions.

system.cpu.commit.fp\_insts 3069053 # Number of committed floating point instructions.

system.cpu.commit.int\_insts 428420357 # Number of committed integer instructions.

system.cpu.commit.function\_calls 6151204 # Number of function calls committed.

system.cpu.commit.op\_class\_0::No\_OpClass 8646356 1.94% 1.94% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntAlu 321159160 72.20% 74.14% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntMult 2406685 0.54% 74.68% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntDiv 0 0.00% 74.68% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatAdd 897130 0.20% 74.88% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatCmp 191234 0.04% 74.93% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatCvt 281149 0.06% 74.99% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMult 204955 0.05% 75.04% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMultAcc 0 0.00% 75.04% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatDiv 60615 0.01% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMisc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatSqrt 4361 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAdd 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAddAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAlu 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdCmp 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdCvt 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMisc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMult 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMultAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShift 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShiftAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSqrt 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatAdd 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatAlu 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatCmp 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatCvt 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatDiv 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMisc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMult 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMultAcc 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatSqrt 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAes 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAesMix 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha1Hash 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha1Hash2 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha256Hash 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSha256Hash2 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShaSigma2 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShaSigma3 0 0.00% 75.05% # Class of committed instruction

system.cpu.commit.op\_class\_0::MemRead 71215561 16.01% 91.06% # Class of committed instruction

system.cpu.commit.op\_class\_0::MemWrite 38336241 8.62% 99.68% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMemRead 573061 0.13% 99.81% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMemWrite 856548 0.19% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::IprAccess 0 0.00% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::total 444833056 # Class of committed instruction

system.cpu.commit.bw\_lim\_events 15570445 # number cycles where commit BW limit reached

system.cpu.rob.rob\_reads 675451280 # The number of ROB reads

system.cpu.rob.rob\_writes 929759411 # The number of ROB writes

system.cpu.timesIdled 1260747 # Number of times that the entire CPU went into an idle state and unscheduled itself

system.cpu.idleCycles 59169898 # Total number of cycles that the CPU has spent unscheduled due to idling

system.cpu.committedInsts 436251113 # Number of Instructions Simulated

system.cpu.committedOps 436251113 # Number of Ops (including micro ops) Simulated

system.cpu.cpi 0.664445 # CPI: Cycles Per Instruction

system.cpu.cpi\_total 0.664445 # CPI: Total CPI of All Threads

system.cpu.ipc 1.505016 # IPC: Instructions Per Cycle

system.cpu.ipc\_total 1.505016 # IPC: Total IPC of All Threads

system.cpu.int\_regfile\_reads 644482126 # number of integer regfile reads

system.cpu.int\_regfile\_writes 342790684 # number of integer regfile writes

system.cpu.fp\_regfile\_reads 3656016 # number of floating regfile reads

system.cpu.fp\_regfile\_writes 1787510 # number of floating regfile writes

system.cpu.misc\_regfile\_reads 1339101 # number of misc regfile reads

system.cpu.misc\_regfile\_writes 308588 # number of misc regfile writes

system.cpu.dcache.tags.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.tags.tagsinuse 972.089741 # Cycle average of tags in use

system.cpu.dcache.tags.total\_refs 109061003 # Total number of references to valid blocks.

system.cpu.dcache.tags.sampled\_refs 2957 # Sample count of references to valid blocks.

system.cpu.dcache.tags.avg\_refs 36882.314170 # Average number of references to valid blocks.

system.cpu.dcache.tags.warmup\_cycle 159000 # Cycle when the warmup percentage was hit.

system.cpu.dcache.tags.occ\_blocks::.cpu.data 972.089741 # Average occupied blocks per requestor

system.cpu.dcache.tags.occ\_percent::.cpu.data 0.949306 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_percent::total 0.949306 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_task\_id\_blocks::1024 1000 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::0 18 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::4 982 # Occupied blocks per task id

system.cpu.dcache.tags.occ\_task\_id\_percent::1024 0.976562 # Percentage of cache occupancy per task id

system.cpu.dcache.tags.tag\_accesses 218132765 # Number of tag accesses

system.cpu.dcache.tags.data\_accesses 218132765 # Number of data accesses

system.cpu.dcache.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.ReadReq\_hits::.cpu.data 69712018 # number of ReadReq hits

system.cpu.dcache.ReadReq\_hits::total 69712018 # number of ReadReq hits

system.cpu.dcache.WriteReq\_hits::.cpu.data 39037446 # number of WriteReq hits

system.cpu.dcache.WriteReq\_hits::total 39037446 # number of WriteReq hits

system.cpu.dcache.LoadLockedReq\_hits::.cpu.data 154290 # number of LoadLockedReq hits

system.cpu.dcache.LoadLockedReq\_hits::total 154290 # number of LoadLockedReq hits

system.cpu.dcache.StoreCondReq\_hits::.cpu.data 154292 # number of StoreCondReq hits

system.cpu.dcache.StoreCondReq\_hits::total 154292 # number of StoreCondReq hits

system.cpu.dcache.demand\_hits::.cpu.data 108749464 # number of demand (read+write) hits

system.cpu.dcache.demand\_hits::total 108749464 # number of demand (read+write) hits

system.cpu.dcache.overall\_hits::.cpu.data 108749464 # number of overall hits

system.cpu.dcache.overall\_hits::total 108749464 # number of overall hits

system.cpu.dcache.ReadReq\_misses::.cpu.data 5805 # number of ReadReq misses

system.cpu.dcache.ReadReq\_misses::total 5805 # number of ReadReq misses

system.cpu.dcache.WriteReq\_misses::.cpu.data 1050 # number of WriteReq misses

system.cpu.dcache.WriteReq\_misses::total 1050 # number of WriteReq misses

system.cpu.dcache.LoadLockedReq\_misses::.cpu.data 3 # number of LoadLockedReq misses

system.cpu.dcache.LoadLockedReq\_misses::total 3 # number of LoadLockedReq misses

system.cpu.dcache.demand\_misses::.cpu.data 6855 # number of demand (read+write) misses

system.cpu.dcache.demand\_misses::total 6855 # number of demand (read+write) misses

system.cpu.dcache.overall\_misses::.cpu.data 6855 # number of overall misses

system.cpu.dcache.overall\_misses::total 6855 # number of overall misses

system.cpu.dcache.ReadReq\_miss\_latency::.cpu.data 402084500 # number of ReadReq miss cycles

system.cpu.dcache.ReadReq\_miss\_latency::total 402084500 # number of ReadReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::.cpu.data 63942485 # number of WriteReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::total 63942485 # number of WriteReq miss cycles

system.cpu.dcache.LoadLockedReq\_miss\_latency::.cpu.data 122500 # number of LoadLockedReq miss cycles

system.cpu.dcache.LoadLockedReq\_miss\_latency::total 122500 # number of LoadLockedReq miss cycles

system.cpu.dcache.demand\_miss\_latency::.cpu.data 466026985 # number of demand (read+write) miss cycles

system.cpu.dcache.demand\_miss\_latency::total 466026985 # number of demand (read+write) miss cycles

system.cpu.dcache.overall\_miss\_latency::.cpu.data 466026985 # number of overall miss cycles

system.cpu.dcache.overall\_miss\_latency::total 466026985 # number of overall miss cycles

system.cpu.dcache.ReadReq\_accesses::.cpu.data 69717823 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.ReadReq\_accesses::total 69717823 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::.cpu.data 39038496 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::total 39038496 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::.cpu.data 154293 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::total 154293 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::.cpu.data 154292 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::total 154292 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.demand\_accesses::.cpu.data 108756319 # number of demand (read+write) accesses

system.cpu.dcache.demand\_accesses::total 108756319 # number of demand (read+write) accesses

system.cpu.dcache.overall\_accesses::.cpu.data 108756319 # number of overall (read+write) accesses

system.cpu.dcache.overall\_accesses::total 108756319 # number of overall (read+write) accesses

system.cpu.dcache.ReadReq\_miss\_rate::.cpu.data 0.000083 # miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_miss\_rate::total 0.000083 # miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::.cpu.data 0.000027 # miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::total 0.000027 # miss rate for WriteReq accesses

system.cpu.dcache.LoadLockedReq\_miss\_rate::.cpu.data 0.000019 # miss rate for LoadLockedReq accesses

system.cpu.dcache.LoadLockedReq\_miss\_rate::total 0.000019 # miss rate for LoadLockedReq accesses

system.cpu.dcache.demand\_miss\_rate::.cpu.data 0.000063 # miss rate for demand accesses

system.cpu.dcache.demand\_miss\_rate::total 0.000063 # miss rate for demand accesses

system.cpu.dcache.overall\_miss\_rate::.cpu.data 0.000063 # miss rate for overall accesses

system.cpu.dcache.overall\_miss\_rate::total 0.000063 # miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_miss\_latency::.cpu.data 69265.202412 # average ReadReq miss latency

system.cpu.dcache.ReadReq\_avg\_miss\_latency::total 69265.202412 # average ReadReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::.cpu.data 60897.604762 # average WriteReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::total 60897.604762 # average WriteReq miss latency

system.cpu.dcache.LoadLockedReq\_avg\_miss\_latency::.cpu.data 40833.333333 # average LoadLockedReq miss latency

system.cpu.dcache.LoadLockedReq\_avg\_miss\_latency::total 40833.333333 # average LoadLockedReq miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::.cpu.data 67983.513494 # average overall miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::total 67983.513494 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::.cpu.data 67983.513494 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::total 67983.513494 # average overall miss latency

system.cpu.dcache.blocked\_cycles::no\_mshrs 1967 # number of cycles access was blocked

system.cpu.dcache.blocked\_cycles::no\_targets 120 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_mshrs 36 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_targets 9 # number of cycles access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_mshrs 54.638889 # average number of cycles each access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_targets 13.333333 # average number of cycles each access was blocked

system.cpu.dcache.writebacks::.writebacks 377 # number of writebacks

system.cpu.dcache.writebacks::total 377 # number of writebacks

system.cpu.dcache.ReadReq\_mshr\_hits::.cpu.data 3147 # number of ReadReq MSHR hits

system.cpu.dcache.ReadReq\_mshr\_hits::total 3147 # number of ReadReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::.cpu.data 753 # number of WriteReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::total 753 # number of WriteReq MSHR hits

system.cpu.dcache.demand\_mshr\_hits::.cpu.data 3900 # number of demand (read+write) MSHR hits

system.cpu.dcache.demand\_mshr\_hits::total 3900 # number of demand (read+write) MSHR hits

system.cpu.dcache.overall\_mshr\_hits::.cpu.data 3900 # number of overall MSHR hits

system.cpu.dcache.overall\_mshr\_hits::total 3900 # number of overall MSHR hits

system.cpu.dcache.ReadReq\_mshr\_misses::.cpu.data 2658 # number of ReadReq MSHR misses

system.cpu.dcache.ReadReq\_mshr\_misses::total 2658 # number of ReadReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::.cpu.data 297 # number of WriteReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::total 297 # number of WriteReq MSHR misses

system.cpu.dcache.LoadLockedReq\_mshr\_misses::.cpu.data 3 # number of LoadLockedReq MSHR misses

system.cpu.dcache.LoadLockedReq\_mshr\_misses::total 3 # number of LoadLockedReq MSHR misses

system.cpu.dcache.demand\_mshr\_misses::.cpu.data 2955 # number of demand (read+write) MSHR misses

system.cpu.dcache.demand\_mshr\_misses::total 2955 # number of demand (read+write) MSHR misses

system.cpu.dcache.overall\_mshr\_misses::.cpu.data 2955 # number of overall MSHR misses

system.cpu.dcache.overall\_mshr\_misses::total 2955 # number of overall MSHR misses

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::.cpu.data 218114000 # number of ReadReq MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::total 218114000 # number of ReadReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::.cpu.data 19044500 # number of WriteReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::total 19044500 # number of WriteReq MSHR miss cycles

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_latency::.cpu.data 120500 # number of LoadLockedReq MSHR miss cycles

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_latency::total 120500 # number of LoadLockedReq MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::.cpu.data 237158500 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::total 237158500 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::.cpu.data 237158500 # number of overall MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::total 237158500 # number of overall MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::.cpu.data 0.000038 # mshr miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::total 0.000038 # mshr miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::.cpu.data 0.000008 # mshr miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::total 0.000008 # mshr miss rate for WriteReq accesses

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_rate::.cpu.data 0.000019 # mshr miss rate for LoadLockedReq accesses

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_rate::total 0.000019 # mshr miss rate for LoadLockedReq accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::.cpu.data 0.000027 # mshr miss rate for demand accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::total 0.000027 # mshr miss rate for demand accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::.cpu.data 0.000027 # mshr miss rate for overall accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::total 0.000027 # mshr miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.data 82059.443190 # average ReadReq mshr miss latency

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::total 82059.443190 # average ReadReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::.cpu.data 64122.895623 # average WriteReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::total 64122.895623 # average WriteReq mshr miss latency

system.cpu.dcache.LoadLockedReq\_avg\_mshr\_miss\_latency::.cpu.data 40166.666667 # average LoadLockedReq mshr miss latency

system.cpu.dcache.LoadLockedReq\_avg\_mshr\_miss\_latency::total 40166.666667 # average LoadLockedReq mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::.cpu.data 80256.683587 # average overall mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::total 80256.683587 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::.cpu.data 80256.683587 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::total 80256.683587 # average overall mshr miss latency

system.cpu.dcache.replacements 1957 # number of replacements

system.cpu.icache.tags.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.cpu.icache.tags.tagsinuse 511.407198 # Cycle average of tags in use

system.cpu.icache.tags.total\_refs 71073776 # Total number of references to valid blocks.

system.cpu.icache.tags.sampled\_refs 1379074 # Sample count of references to valid blocks.

system.cpu.icache.tags.avg\_refs 51.537319 # Average number of references to valid blocks.

system.cpu.icache.tags.warmup\_cycle 77000 # Cycle when the warmup percentage was hit.

system.cpu.icache.tags.occ\_blocks::.cpu.inst 511.407198 # Average occupied blocks per requestor

system.cpu.icache.tags.occ\_percent::.cpu.inst 0.998842 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_percent::total 0.998842 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_task\_id\_blocks::1024 512 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::0 86 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::3 3 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::4 423 # Occupied blocks per task id

system.cpu.icache.tags.occ\_task\_id\_percent::1024 1 # Percentage of cache occupancy per task id

system.cpu.icache.tags.tag\_accesses 143626654 # Number of tag accesses

system.cpu.icache.tags.data\_accesses 143626654 # Number of data accesses

system.cpu.icache.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.cpu.icache.ReadReq\_hits::.cpu.inst 69694702 # number of ReadReq hits

system.cpu.icache.ReadReq\_hits::total 69694702 # number of ReadReq hits

system.cpu.icache.demand\_hits::.cpu.inst 69694702 # number of demand (read+write) hits

system.cpu.icache.demand\_hits::total 69694702 # number of demand (read+write) hits

system.cpu.icache.overall\_hits::.cpu.inst 69694702 # number of overall hits

system.cpu.icache.overall\_hits::total 69694702 # number of overall hits

system.cpu.icache.ReadReq\_misses::.cpu.inst 1429088 # number of ReadReq misses

system.cpu.icache.ReadReq\_misses::total 1429088 # number of ReadReq misses

system.cpu.icache.demand\_misses::.cpu.inst 1429088 # number of demand (read+write) misses

system.cpu.icache.demand\_misses::total 1429088 # number of demand (read+write) misses

system.cpu.icache.overall\_misses::.cpu.inst 1429088 # number of overall misses

system.cpu.icache.overall\_misses::total 1429088 # number of overall misses

system.cpu.icache.ReadReq\_miss\_latency::.cpu.inst 52968219999 # number of ReadReq miss cycles

system.cpu.icache.ReadReq\_miss\_latency::total 52968219999 # number of ReadReq miss cycles

system.cpu.icache.demand\_miss\_latency::.cpu.inst 52968219999 # number of demand (read+write) miss cycles

system.cpu.icache.demand\_miss\_latency::total 52968219999 # number of demand (read+write) miss cycles

system.cpu.icache.overall\_miss\_latency::.cpu.inst 52968219999 # number of overall miss cycles

system.cpu.icache.overall\_miss\_latency::total 52968219999 # number of overall miss cycles

system.cpu.icache.ReadReq\_accesses::.cpu.inst 71123790 # number of ReadReq accesses(hits+misses)

system.cpu.icache.ReadReq\_accesses::total 71123790 # number of ReadReq accesses(hits+misses)

system.cpu.icache.demand\_accesses::.cpu.inst 71123790 # number of demand (read+write) accesses

system.cpu.icache.demand\_accesses::total 71123790 # number of demand (read+write) accesses

system.cpu.icache.overall\_accesses::.cpu.inst 71123790 # number of overall (read+write) accesses

system.cpu.icache.overall\_accesses::total 71123790 # number of overall (read+write) accesses

system.cpu.icache.ReadReq\_miss\_rate::.cpu.inst 0.020093 # miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_miss\_rate::total 0.020093 # miss rate for ReadReq accesses

system.cpu.icache.demand\_miss\_rate::.cpu.inst 0.020093 # miss rate for demand accesses

system.cpu.icache.demand\_miss\_rate::total 0.020093 # miss rate for demand accesses

system.cpu.icache.overall\_miss\_rate::.cpu.inst 0.020093 # miss rate for overall accesses

system.cpu.icache.overall\_miss\_rate::total 0.020093 # miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_miss\_latency::.cpu.inst 37064.351530 # average ReadReq miss latency

system.cpu.icache.ReadReq\_avg\_miss\_latency::total 37064.351530 # average ReadReq miss latency

system.cpu.icache.demand\_avg\_miss\_latency::.cpu.inst 37064.351530 # average overall miss latency

system.cpu.icache.demand\_avg\_miss\_latency::total 37064.351530 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::.cpu.inst 37064.351530 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::total 37064.351530 # average overall miss latency

system.cpu.icache.blocked\_cycles::no\_mshrs 3399 # number of cycles access was blocked

system.cpu.icache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_mshrs 35 # number of cycles access was blocked

system.cpu.icache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_mshrs 97.114286 # average number of cycles each access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.icache.writebacks::.writebacks 1378562 # number of writebacks

system.cpu.icache.writebacks::total 1378562 # number of writebacks

system.cpu.icache.ReadReq\_mshr\_hits::.cpu.inst 50013 # number of ReadReq MSHR hits

system.cpu.icache.ReadReq\_mshr\_hits::total 50013 # number of ReadReq MSHR hits

system.cpu.icache.demand\_mshr\_hits::.cpu.inst 50013 # number of demand (read+write) MSHR hits

system.cpu.icache.demand\_mshr\_hits::total 50013 # number of demand (read+write) MSHR hits

system.cpu.icache.overall\_mshr\_hits::.cpu.inst 50013 # number of overall MSHR hits

system.cpu.icache.overall\_mshr\_hits::total 50013 # number of overall MSHR hits

system.cpu.icache.ReadReq\_mshr\_misses::.cpu.inst 1379075 # number of ReadReq MSHR misses

system.cpu.icache.ReadReq\_mshr\_misses::total 1379075 # number of ReadReq MSHR misses

system.cpu.icache.demand\_mshr\_misses::.cpu.inst 1379075 # number of demand (read+write) MSHR misses

system.cpu.icache.demand\_mshr\_misses::total 1379075 # number of demand (read+write) MSHR misses

system.cpu.icache.overall\_mshr\_misses::.cpu.inst 1379075 # number of overall MSHR misses

system.cpu.icache.overall\_mshr\_misses::total 1379075 # number of overall MSHR misses

system.cpu.icache.ReadReq\_mshr\_miss\_latency::.cpu.inst 49439003000 # number of ReadReq MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_latency::total 49439003000 # number of ReadReq MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::.cpu.inst 49439003000 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::total 49439003000 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::.cpu.inst 49439003000 # number of overall MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::total 49439003000 # number of overall MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_rate::.cpu.inst 0.019390 # mshr miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_mshr\_miss\_rate::total 0.019390 # mshr miss rate for ReadReq accesses

system.cpu.icache.demand\_mshr\_miss\_rate::.cpu.inst 0.019390 # mshr miss rate for demand accesses

system.cpu.icache.demand\_mshr\_miss\_rate::total 0.019390 # mshr miss rate for demand accesses

system.cpu.icache.overall\_mshr\_miss\_rate::.cpu.inst 0.019390 # mshr miss rate for overall accesses

system.cpu.icache.overall\_mshr\_miss\_rate::total 0.019390 # mshr miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::.cpu.inst 35849.393978 # average ReadReq mshr miss latency

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::total 35849.393978 # average ReadReq mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::.cpu.inst 35849.393978 # average overall mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::total 35849.393978 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::.cpu.inst 35849.393978 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::total 35849.393978 # average overall mshr miss latency

system.cpu.icache.replacements 1378562 # number of replacements

system.membus.snoop\_filter.tot\_requests 2762552 # Total number of requests made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_requests 1380519 # Number of requests hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_requests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.snoop\_filter.tot\_snoops 0 # Total number of snoops made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_snoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_snoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.pwrStateResidencyTicks::UNDEFINED 144932423500 # Cumulative time (in ticks) in various power states

system.membus.trans\_dist::ReadResp 1381734 # Transaction distribution

system.membus.trans\_dist::WritebackDirty 377 # Transaction distribution

system.membus.trans\_dist::WritebackClean 1378562 # Transaction distribution

system.membus.trans\_dist::CleanEvict 1580 # Transaction distribution

system.membus.trans\_dist::ReadExReq 293 # Transaction distribution

system.membus.trans\_dist::ReadExResp 293 # Transaction distribution

system.membus.trans\_dist::ReadCleanReq 1379075 # Transaction distribution

system.membus.trans\_dist::ReadSharedReq 2661 # Transaction distribution

system.membus.trans\_dist::InvalidateReq 4 # Transaction distribution

system.membus.pkt\_count\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 4136711 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 7868 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count::total 4144579 # Packet count per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 176488704 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 213120 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size::total 176701824 # Cumulative packet size per connected master and slave (bytes)

system.membus.snoops 0 # Total snoops (count)

system.membus.snoopTraffic 0 # Total snoop traffic (bytes)

system.membus.snoop\_fanout::samples 1382033 # Request fanout histogram

system.membus.snoop\_fanout::mean 0 # Request fanout histogram

system.membus.snoop\_fanout::stdev 0 # Request fanout histogram

system.membus.snoop\_fanout::underflows 0 0.00% 0.00% # Request fanout histogram

system.membus.snoop\_fanout::0 1382033 100.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::1 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::2 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::overflows 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::min\_value 0 # Request fanout histogram

system.membus.snoop\_fanout::max\_value 0 # Request fanout histogram

system.membus.snoop\_fanout::total 1382033 # Request fanout histogram

system.membus.reqLayer0.occupancy 8418940000 # Layer occupancy (ticks)

system.membus.reqLayer0.utilization 5.8 # Layer utilization (%)

system.membus.respLayer1.occupancy 7007623199 # Layer occupancy (ticks)

system.membus.respLayer1.utilization 4.8 # Layer utilization (%)

system.membus.respLayer2.occupancy 15982997 # Layer occupancy (ticks)

system.membus.respLayer2.utilization 0.0 # Layer utilization (%)

---------- End Simulation Statistics ----------